THE INSTITUTION OF ENGINEERS, SRI LANKA
IESL ENGINEERING COURSE

PART III(A) EXAMINATION—NOVEMBER 2008
309 ELECTRONICS

Instructions: Answer five questions only. Tentative mark allocation for each part is shown in brackets for guidance only.

Time: Three hours.

Q1. (a) Why should the use of inductors in modern electronic circuits be avoided if possible? [3 marks]
   (b) List two parameters, and their importance of commercially available operational amplifiers that affect the design of active filters. [3 marks]
   (c) For the second order low-pass section shown in Fig. Q1(c) show that

   \[
   \frac{A_v(s)}{A_{v_o}} = \frac{1}{(RCs)^2 + (3 - A_{v_o})RCs + 1},
   \]

   where \( A_{v_o} \) is the mid-band gain, and \( A_v = \frac{v_o}{v_s} \). Use the symbols, \( v' \) and \( v_f \) given in the figure, in your calculations. [6 marks]

![Figure Q1(c): Second order section.](image)

(d) Design a third-order Butterworth low-pass filter having a mid-band gain of 1, using the second-order section in Fig. Q1(c) and other circuitry as necessary. Choose \( R_1 = 10 \, k\Omega \) and \( C = 0.1 \, \mu F \). The third-order, normalized Butterworth polynomial is \((s + 1)(s^2 + s + 1)\). [8 marks]

Q2. (a) Draw the transfer characteristic curves for an ideal comparator and a non-ideal comparator, and explain the comparison action. [6 marks]
   (b) An inverting Schmitt trigger circuit is shown in Fig. Q2(b).
   i. Draw the transfer characteristics. [8 marks]
   ii. Explain the hysteresis observed in the transfer characteristics.
iii. Draw the output waveform if an input voltage of \( u_i(t) = 2\sin(10\pi t) \) V is applied. Assume that the output voltage \( V_0 = V_Z + V_D = 7 \) V, when the zener diodes are considered. \( V_D \) is the forward biased voltage of a Zener diode.

(c) Draw the circuit diagram of a free-running square waveform generator using a Schmitt trigger circuit and other passive elements. [6 marks]

Q3. (a) Show the collector current waveforms and conduction angles for classes A, B, AB, and C output stages. [4 marks]

(b) Fig. Q3(b) shows a portion of a typical operational amplifier including the output stage (Q1 and Q2). \( V \) is an adjustable voltage difference. Do you expect a significant crossover distortion in this stage? Reason out your answer. [6 marks]

(c) A class B push-pull stage delivers 16 W to an 8-\( \Omega \) load. It uses a \( \pm 20 \) V supply. Deriving necessary formulae, determine the following: [10 marks]

i. Peak current drawn from each supply
ii. Total supply power
iii. Power conversion efficiency
iv. Maximum power each transistor must be able to dissipate

Q4. (a) What is the purpose of voltage regulation? [3 marks]
(b) When the input to a particular voltage regulator is decreased by 5 V, the output decreases by 0.25 V. The nominal output is 20 V. When there is a full-load current of 10 mA, the output voltage is 19.9 V. Compute the line regulation, and the voltage regulation as a percentage change from no-load to full-load. [5 marks]
(c) A series voltage regulator is shown in Fig. Q4(c). $Q_1$ is a power transistor. [12 marks]

![Series regulator diagram]

Figure Q4(c): Series regulator.

i. Explain the voltage regulation action when $R_L$ is increased, and when $V_{IN}$ is decreased.
ii. Find the output voltage with no-load condition.
iii. Determine the maximum current that the regulator provides to a load.

Q5. (a) Show the basic construction, two-transistor equivalent circuit, and the characteristic curves of a SCR, and explain the turning-on and turning-off operations. [5 marks]
(b) In the circuit of Fig. Q5(b) a triac is used to control the power supplied to the load. Explain the operation of the circuit. How would you control the conduction angle? [7 marks]

![Triac power controller diagram]

Figure Q5(b): Triac power controller.

(c) A relaxation oscillator using a UJT is shown in Fig. Q5(c). [8 marks]
i. Draw the $v_G$ and $v_{R_2}$ waveforms, and show that, for UJT turn-on and turn-off,
\[
\frac{V_{BB} - V_P}{I_P} > R_1 > \frac{V_{BB} - V_V}{I_V},
\]
where $V_P$ is the peak point voltage, $V_V$ is the valley point voltage, and $I_P$ and $I_V$ are the corresponding $I_E$ values, respectively.

ii. Determine the value of $R_1$ that will ensure proper turn-on and turn-off of the UJT if $\eta = \frac{T_{B1}}{r_{BB}} = 0.5$, $V_V = 1$ V, $I_V = 10$ mA, $I_P = 20$ $\mu$A, and $V_P = 14$ V.

Q6. (a) Show the basic configuration of the three programmable logic devices, PROM, PAL, and PLA. Use these configurations to rank them in terms of flexibility. [5 marks]

(b) Design a two-bit adder using a ROM. Indicate the size of the ROM. [5 marks]

(c) Implement the following Boolean functions using a PLA. Show the Karnaugh maps, the two functions that use a minimum number of product terms, the PLA programming table, and the PLA fuse map. [10 marks]

$$F_1(A, B, C) = \sum(0, 1, 2, 4). \quad F_2(A, B, C) = \sum(0, 5, 6, 7).$$

Q7. (a) Show using a circuit diagram how a four-bit digital to analog converter (DAC) can be built using a summing amplifier. [6 marks]

(b) Using a block diagram explain why several important types of analog to digital converters (ADCs) utilize a DAC as a part of their circuitry. [6 marks]

(c) A 10-bit digital ramp ADC has a full-scale output of 10.23 V. Its clock frequency is 1 MHz.

i. Determine the digital equivalent obtained for an analog input voltage of 3.728 V.

ii. Compute the conversion time.
Q8. (a) Explain the operation of a computer by outlining the functions of the units in the block diagram in Fig. Q8(a).

(b) Fig. Q8(b) shows a CPU driving a static memory.

i. How many memory locations does the memory chip have?
ii. Explain the function of the multiplexer.
iii. What is the advantage of using this configuration?

(c) Some typical instructions and the corresponding opcodes of a processor are given in Table 1. Table 2 lists a sequence of instructions. Assuming that all instructions except HLT are two byte instructions, find the values in memory locations and the accumulator after each of the instructions in Table 2 is executed.
Table 1: Mnemonics and opcodes.

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Opcode (Hex)</th>
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<tbody>
<tr>
<td>LDA</td>
<td>5B</td>
</tr>
<tr>
<td>ADD</td>
<td>6D</td>
</tr>
<tr>
<td>SUM</td>
<td>A2</td>
</tr>
<tr>
<td>STA</td>
<td>8A</td>
</tr>
<tr>
<td>JMP</td>
<td>4C</td>
</tr>
<tr>
<td>JPZ</td>
<td>76</td>
</tr>
<tr>
<td>HLT</td>
<td>3F</td>
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Table 2: A sequence of instruction in memory.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Memory address</th>
<th>Memory word</th>
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<td>5B</td>
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<td>01</td>
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<tr>
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