THE INSTITUTION OF ENGINEERS, SRI LANKA
IESL ENGINEERING COURSE

PART III EXAMINATION—JUNE 2010

309 ELECTRONICS

Instructions: This question paper contains eight questions in 5 pages. Answer **five** questions **only**. Tentative mark allocation for each part is shown in brackets for guidance only. **Time:** Three hours.

Q1. (a) List commonly used filter transfer functions and their characteristics. **[4 marks]**

(b) A second order stage is shown in Figure 1, where v_I is the input voltage and v_O is the output voltage. Show that its transfer function is **[6 marks]**

$$A(s) = -\frac{\frac{R_2}{R_1}}{1 + C_1\left(R_2 + R_3 + \frac{R_2 R_3}{R_1}\right)s + C_1 C_2 R_2 R_3 s^2}.$$

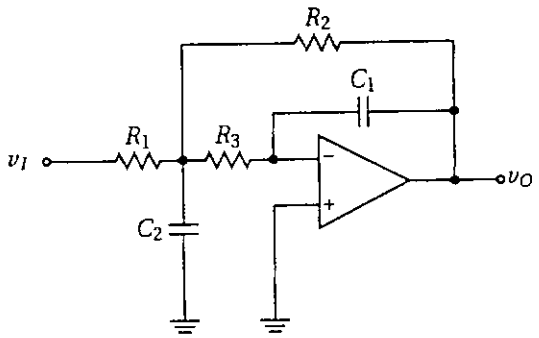

Figure 1: Circuit for **Q1**b.

(c) Use the second order stage in Figure 1 and other circuitry as necessary to design a third-order unity-gain Butterworth low-pass filter with a corner frequency of $f_C = 50\,\text{kHz}$. You may use only 22 pF and 1 nF capacitors. Butterworth coefficients for the third-order filter are **[10 marks]**

Order n	Stage i	a_i	b_i
3	1	1.0000	0.0000
	2	1.0000	1.0000

for a transfer function of a stage of the form

$$A_i(s) = \frac{A_o}{1 + a_i s + b_i s^2}.$$

Q2. (a) Sketch the circuit diagrams of the non-inverting and inverting bistable multivibrators along with their voltage transfer characteristics. **[6 marks]**

(b) Sketch the circuit diagram of a free-running triangular waveform generator. **[4 marks]**

(c) Figure 2 shows a one shot circuit. The operational amplifier is supplied with voltage levels L_+ and L^-. In the stable state, $v_O = L^+$, $v_A = 0$, and $v_B = -V_{\text{ref}}$. The circuit is triggered by applying a positive input pulse of height greater than V_{ref}. Assume that $C_1 R_1 \ll CR$. **[10 marks]**

i. Sketch the waveforms v_A, and v_O along with the trigger pulse.

ii. What is the width T of the pulse generated at the output?

iii. How would you control the pulse width T?

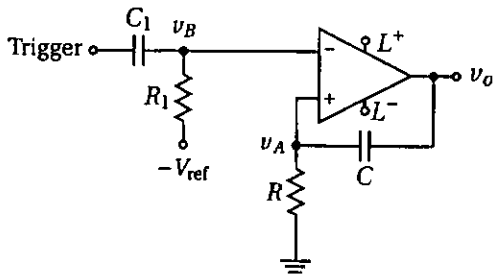

Figure 2: Circuit for **Q2**c.

Q3. (a) Figure 3 shows a simple common-emitter amplifier. $V_{CC} = 20\,\text{V}$ and $R_C = 140\,\Omega$. **[6 marks]**

i. If there are two transistors with total power dissipation 0.4 W, and 0.6 W, what would you select?

ii. In regard to the transistor power dissipation, how would you accommodate a substantial change in the ambient temperature without replacing the transistor?

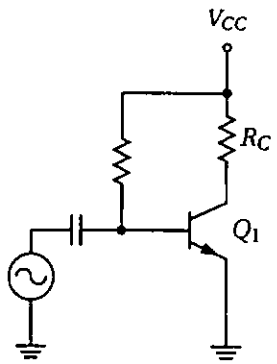

Figure 3: Circuit for **Q3**a.

(b) A class B power amplifier stage is to be designed to deliver an average power of 20 W to an 8-Ω load. The power supply voltage V_{CC} is to be 5 V greater than the peak output voltage. **[8 marks]**

i. Compute the average power drawn from each supply.

ii. Compute the power conversion efficiency and compare with the maximum efficiency.

iii. Determine the maximum power each transistor should be able to dissipate.

iv. Why is the supply voltage selected to be 5 V greater than the peak output voltage?

(c) Figure 4 shows an output stage. Identify its type and provide a short-circuit protection mechanism for this output stage. **[6 marks]**

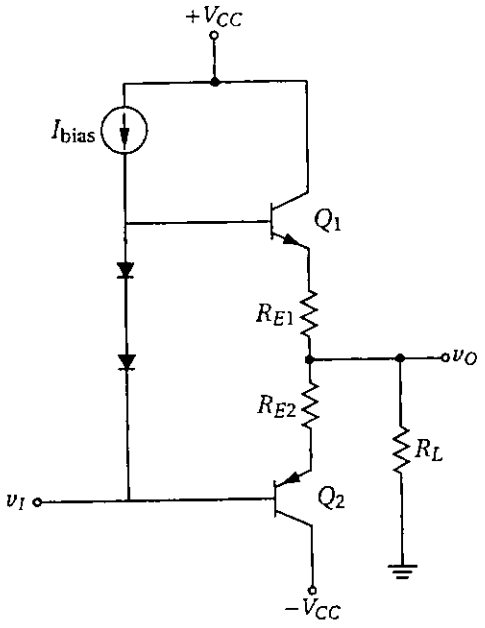

Figure 4: Circuit for **Q3c**.

Q4. (a) Compare unregulated and regulated power supplies paying special attention to the operating principle of regulated power supplies. **[6 marks]**

(b) A regulator circuit is shown in Figure 5 with $V_{ref} = 7.15\,V$. Give a step-by-step explanation of its operation and compute its output voltage and maximum current. **[8 marks]**

(c) The circuit in Figure 5 does not have over voltage protection. Provide an over voltage crowbar protection and explain what happens when the output exceeds the maximum voltage. **[6 marks]**

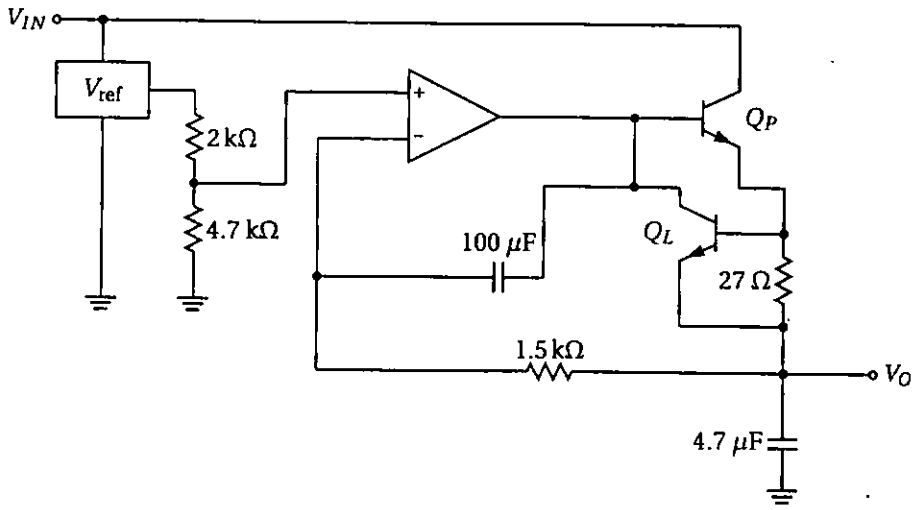

Figure 5: Circuit for **Q4**b.

Q5. (a) Describe the characteristics and applications of the SCR, diac, triac, and UJT. Show sketches of I-V characteristics. **[8 marks]**

(b) The triac in the power controller circuit shown in Figure 6 has an anode-cathode voltage drop of 1 V when it is conducting. If $R_L = 30\Omega$, find the rms value of v_{in} that is necessary if it is required to deliver an average power of 100 W to R_L when the firing angle is 45°? **[6 marks]**

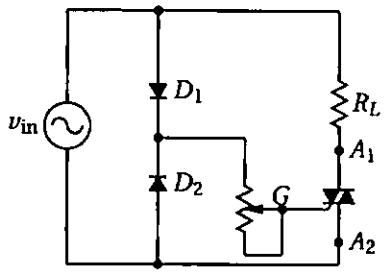

Figure 6: Circuit for **Q5**b.

(c) An SCR with a forward break over voltage $V_{BR(F)} = 10$ V is supplied by a sawtooth waveform of peak amplitude 30 V (Figure 7) though a 50-Ω resistor. When conducting, the anode-cathode voltage drop of the SCR is 1 V. Find the average current in R_L. **[6 marks]**

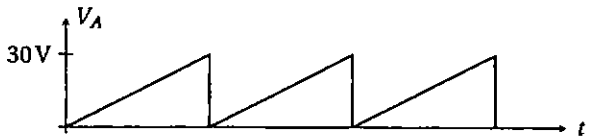

Figure 7: Circuit for **Q5**c.

Q6. (a) A 32×6 ROM converts a six-bit binary number to its corresponding two-digit binary-coded decimal (BCD) number. Note that to represent six-bit binary numbers as BCD, at least seven bits as required. Design the system and specify the truth-table for the ROM. **[6 marks]**

(b) Consider the following Boolean functions: **[8 marks]**

$$w(A,B,C,D) = \sum(2,12,13)$$
$$x(A,B,C,D) = \sum(7,8,9,10,11,12,13,14,15)$$
$$y(A,B,C,D) = \sum(0,2,3,4,5,6,7,8,10,11,15)$$
$$z(A,B,C,D) = \sum(1,2,8,12,13)$$

Simplify, and implement these using a PAL. Show the PAL programming table and the fuse map.

(c) FPGAs are known to be very versatile and widely used. Describe the reason for this trend by mentioning the advantages of FPGAs. **[6 marks]**

Q7. (a) Consider the following signal

$$v(t) = 5\sin(2\pi f) + 5 \quad \text{V}.$$

where $f = 10\,\text{kHz}$. It is sampled at $f_s = 12\,\text{kHz}$ and each sample is quantized into 5 bits. **[8 marks]**

i. Sketch two cycles of the input waveform along with the waveform reconstructed from the quantized samples.

ii. How would you solve the main problem in the aforementioned process?

iii. If the sampled voltage value needs to be wrong by no more than 0.5 mV, how many bits per sample would be required?

(b) Explain how dual-slope integration ADCs avoid some problems in single-slope integration ADCs. **[4 marks]**

(c) An 8-bit successive approximation register ADC with a full-range input voltage of 10 V is presented with an input voltage of 7.1 V. List the sequence of digital outputs until the output settles down. **[8 marks]**

Q8. (a) Sketch a block diagram of a computer clearly indicating the data and control paths, and describe the operation. **[6 marks]**

(b) Using a sketch show how a 2048-byte memory can be constructed using 128×8-bit chips. Clearly indicate the number of address lines, and how they are connected to the chips. **[6 marks]**

(c) Arithmetic and logic operations in a microprocessor are handled by the ALU which is a combinational circuit. Using sketches of these circuits show how the operations, AND, addition, and subtraction are done in an ALU. **[8 marks]**