THE INSTITUTION OF ENGINEERS, SRI LANKA

PART III REPEAT EXAMINATION- OCTOBER 2013

309 ELECTRONIC SYSTEMS ENGINEERING

Answer **FIVE** questions only

Time allowed: 3 Hours

Q1.

(a) List three commonly used filter transfer functions and their characteristics.

(6Marks)

(b)

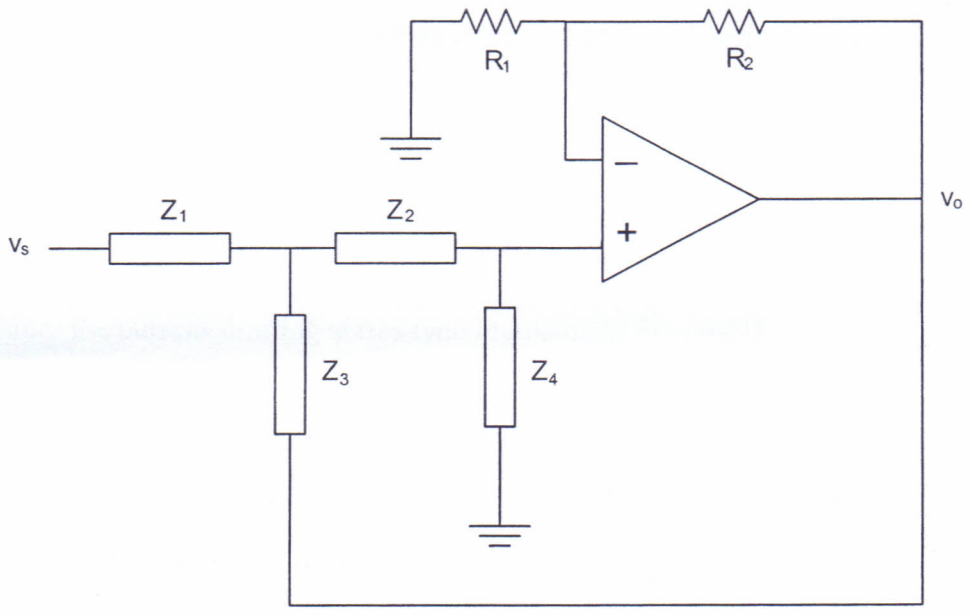

Figure-Q1

i. Derive the transfer function of the active filter circuit shown in Figure-Q1.

(8Marks)

ii. Let $Z1 = Z2$ and $Z3 = Z4$. Select the suitable component values to design a second order Butterworth high pass filter with a cutoff frequency $200kHz$.

(6Marks)

Hint: Second order high pass Butterworth filter transfer function:

$$H(s) = \frac{K_1 s^2}{s^2 + K_2 s + K_3}$$

Q2.

(a) Compare the structures of ROM, PLA and PAL. **(6Marks)**

(b) A line following robot has to be designed with the following specifications.

- Robot has four sensors in a fixed array with the spacing between the sensors such that at most 3 sensors will be on the line at a time. On the other hand, there can be instances with a minimum of only one outer sensor on the line.
- Whenever the two center sensors are on the line, the robot should be moved forward; otherwise turning should be carried out to align the robot with the line. When the robot meets end of the line it should stop.
- Robot has two independent motors (connected to wheels) to generate motion.
  - Bothe motors on→ Forward motion
  - Left motor on, right motor off → Right turn
  - Left motor off, right motor on→ Left turn
  - Both motors off→ No motion.

A digital combinational control circuit takes the sensor outputs' logical values as inputs and outputs logic signals to the motors.

i. Define the different inputs and outputs with suitable logic values. Hence, draw the truth table and derive the simplified logic expressions. **(8Marks)**

ii. Implement the circuit using an appropriate PLA. **(6Marks)**

Q3.

(a) Compare successive approximation type, flash and counter type ADCs focusing on their conversion speed, resolution and cost. **(6Marks)**

(b) Using suitable diagrams, explain the operation of a counter type ADC. **(5Marks)**

(c) A certain counter type ADC has a counter output consisting of 8 bits and a full scale DAC output of $8V$. Find,

i. The resolution of the ADC. **(3Marks)**

ii. Digital output obtained for an input of $2.75V$. **(3Marks)**

iii. Minimum frequency of the clock signal to have a guaranteed conversion within 1ms. **(3Marks)**

Q4.

(a) Show the output waveforms and conduction angles of different classes of power amplifiers. **(6Marks)**

(b) Class B power amplifiers provide a better efficiency than Class A. Discuss a main disadvantage of Class B over Class A. Further discuss a method to overcome the above disadvantage. **(5Marks)**

(c) A Class B push-pull power amplifier delivers $16W$ to a 8Ω load. It uses a $\pm 20V$ DC power supply. Determine,

i. Peak current drawn from each supply. **(2Marks)**
ii. Total power supplied to the circuit. **(2Marks)**
iii. Power efficiency. **(2Marks)**
iv. Maximum power dissipation capability for each transistor. **(3Marks)**

Q5.

(a) Draw the basic block diagram of a DC power supply highlighting the need for regulation. **(5Marks)**

(b) What are the advantages of switching regulation over series or shunt regulation? **(5Marks)**

(c) Consider the current limiting series type regulator in Figure-Q5.

i. Explain the circuit behavior when V_{in} is decreased. **(3Marks)**
ii. Explain the circuit behavior when R_L is increased. **(3Marks)**
iii. Let the load voltage to be maintained at $6V$. Further assume that both T1 and T2 are Si transistors. Find V. Hence find the maximum load current allowed in this circuit. (Clearly state all your assumptions) **(4Marks)**

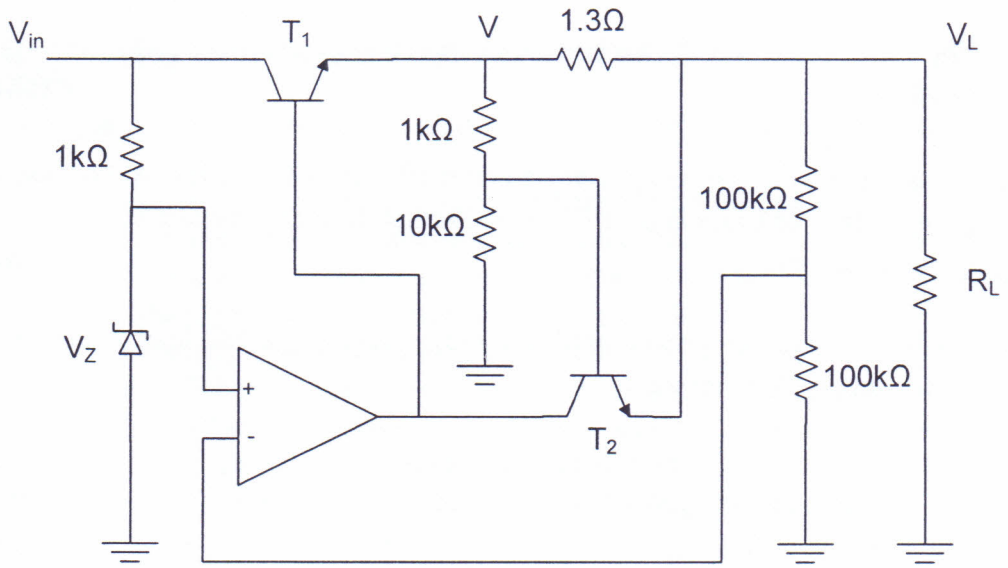

Figure-Q5

Q6.

(a) Describe the operation of SCR, DIAC and TRIAC with the help of their I-V characteristic curves. **(6Marks)**

(b)

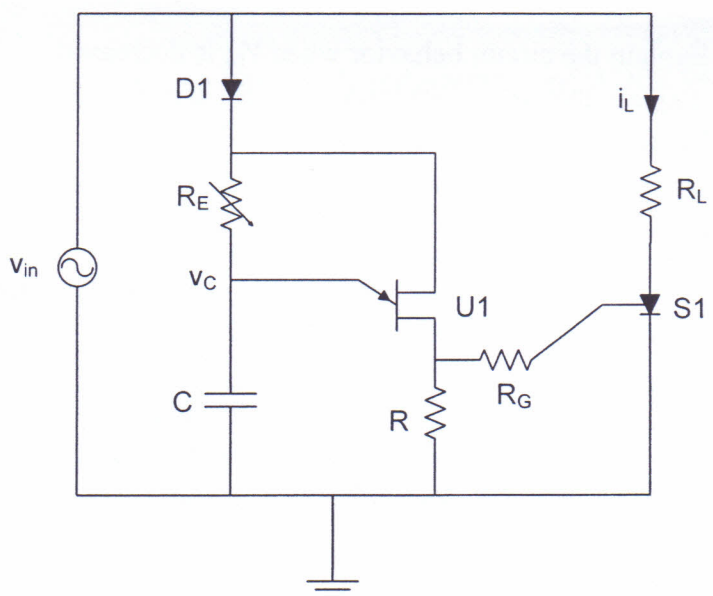

Figure-Q6

In the circuit shown in Figure-Q6, U1 UJT provides a trigger operation to the SCR S1. Assume the drop across the SCR is negligible. Further, v_{in} is sinusoidal with $20V\ rms$ and $R_L = 20\Omega$.

i. Explain the operation of the circuit with the help of waveforms of v_{in}, v_C and i_L. **(6Marks)**

ii. What is the maximum possible power that can be delivered to the load? **(4Marks)**

iii. Find the maximum load power delivered for a SCR firing angle of 45^0. **(4Marks)**

Q7.

(a) Draw the transfer characteristic curves for ideal and non-ideal comparators and compare them. **(4Marks)**

(b) The one shot circuit shown in Figure-Q7 is having $v_O = L+$, $v_A = 0$ and $v_B = -V_{Ref}$ in the stable state. The circuit is triggered by applying a positive input pulse greater than V_{Ref}. Assume that $R_1C_1 \ll RC$.

i. Sketch the waveforms of v_A and v_O along with the trigger pulse. **(4Marks)**

ii. What is the width of the pulse (T) generated at the output? **(4Marks)**

iii. Explain how T can be controlled. **(3Marks)**

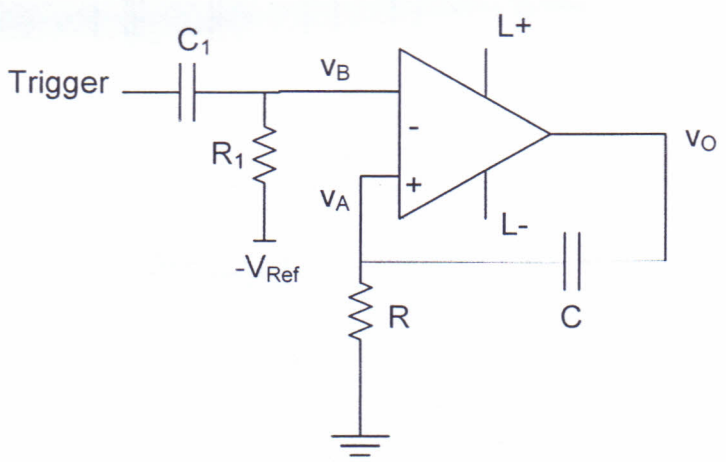

Figure-Q7

(c) Draw the circuit diagram of a free running square wave generator using a Schmitt trigger circuit. **(5Marks)**

Q8.

(a) Sketch a basic level block diagram of computer's components. Include the interconnection bus system clearly showing different types of signals flow in each. **(6Marks)**

(b) Construct a 64Kx16 (64K words with word size 16 bits) ROM using 16Kx8 (16K words with word size 8 bits) ROM chips. You have to clearly show the interconnection lines and their widths. **(6Marks)**

(c) A basic level micro processor control unit is to be designed according to the following specifications.

- Operations: Addition, logical AND, logical OR, bitwise inversion, increment by one.
- Operations to be performed on data stored in A and B registers accordingly.
- Results of the ALU operation to be stored in register C.
- Current instruction is loaded to the instruction register (IR).

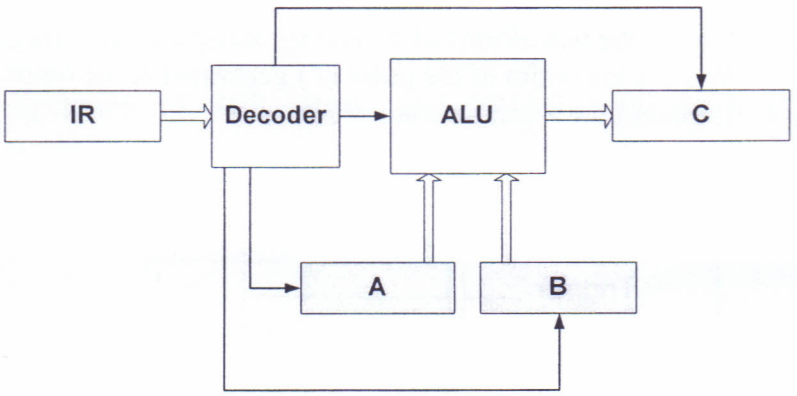

Figure-Q8

i. Design the circuitry inside the ALU. **(4Marks)**

ii. Design the combinational circuit in the decoder. **(4Marks)**

(Clearly state all your assumptions and show all the design steps)