THE INSTITUTION OF ENGINEERS, SRI LANKA
IESL ENGINEERING COURSE

PART II EXAMINATION – JULY 2012

210 ELECTRONICS

Instructions: This question paper contains eight questions in ten pages. Answer **five** questions **only**. Tentative mark allocation for each part is shown in brackets for guidance only.

Time: Three hours.

Question 01

a) Sketch and label the typical V-I characteristic of a typical diode and indicate the breakdown voltage, reverse saturation current, cutting voltage, knee current, rectifier diode region and zener diode region.

[6 marks]

b) Consider the circuit of Figure Q.1 (b). The capacitors are very large, so they discharge only a very small amount per cycle. Sketch the voltage at point A vs. time .Find the voltage across the load. What is the peak inverse voltage across each diode?

[6 marks]

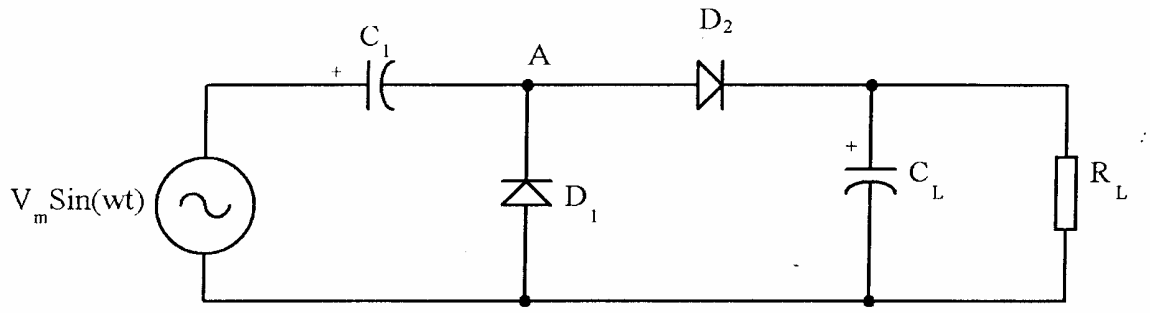

Figure Q.1 (b)

c) In the circuit shown in Figure Q.1 (c) the zener diode is used to protect the Galvanometer which has 200μA fall scale rating and 560Ω internal resistance. It should show full deflection when $V_i = 20v$ and if V_i is increased beyond 20v, the current in the galvanometer should remain constant at 200 μA. Find the value of R_1 and R_2.

[8 marks]

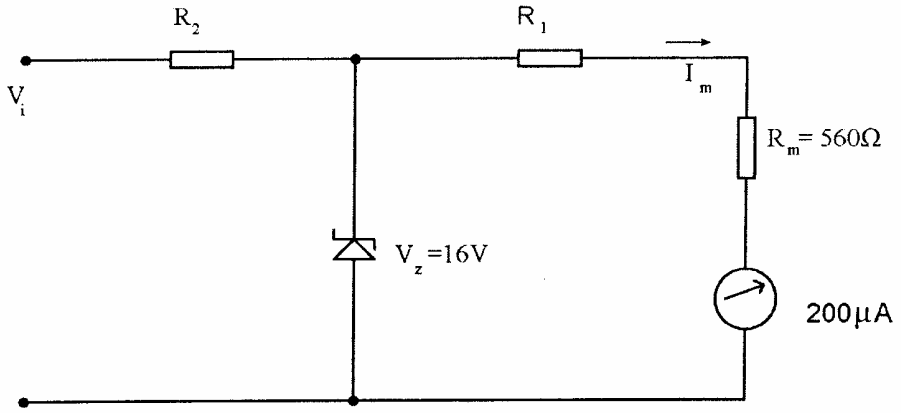

Figure Q.1 (c)

Question 02

a) Explain the function of each component (R_1, R_2, R_C, R_e, C_1, C_2 and C_e) as shown in the Figure Q.2 (a).

[6 marks]

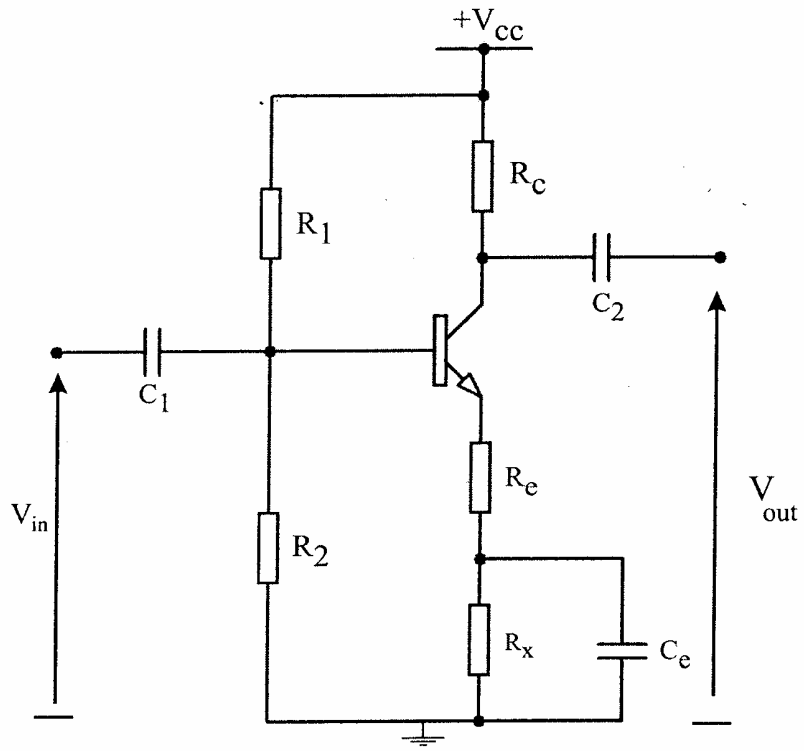

Figure Q.2 (a)

b) Consider the circuit shown in Figure Q.2 (b). Find R_1 and R_C, if a bias point of V_{CE}=5V and I_C =2mA is required.

[6 marks]

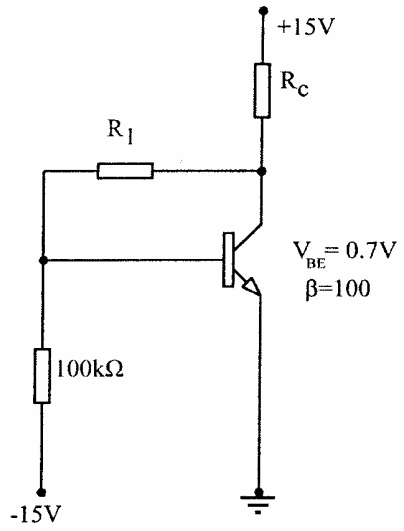

Figure Q.2 (b)

c) Consider the common-emitter amplifier of Figure Q.2(c). Draw the DC equivalent circuit and find I_{CQ}. Find the value of r_π. Then calculate values for A_v, A_{vo}, Z_{in}, A_i, G and Z_o. Assume operation is in the mid-band region for which the coupling and bypass capacitors are short circuits.

[8 marks]

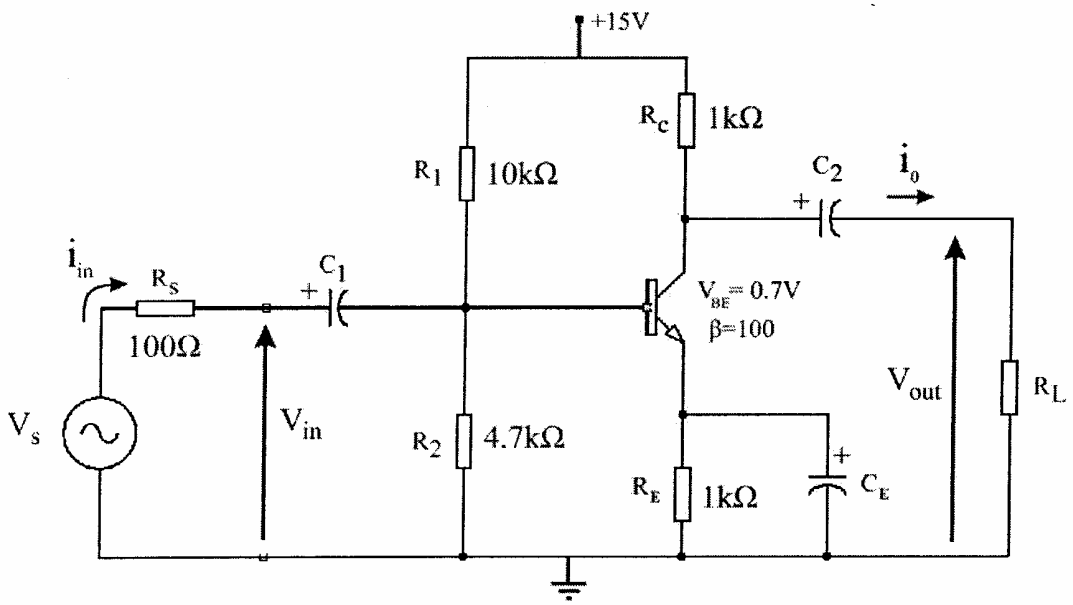

Figure Q.2(c)

Question 03:

a) List the characteristics of an ideal Op-Amp and define the term common mode rejection ratio (CMRR) of a differential amplifier. Why is it desirable for an Op-Amp to have a CMRR?

[6 marks]

b) Figure Q.3 (b) shows a version of the inverting amplifier that can have high gain magnitude. Derive an expression for the voltage gain under the ideal op amp assumption. Also, find the input impedance and output impedance. Evaluate the results for $R_1 = R_3 =$ 1kΩ and $R_2 = R_4 = 10$ kΩ.

[6 marks]

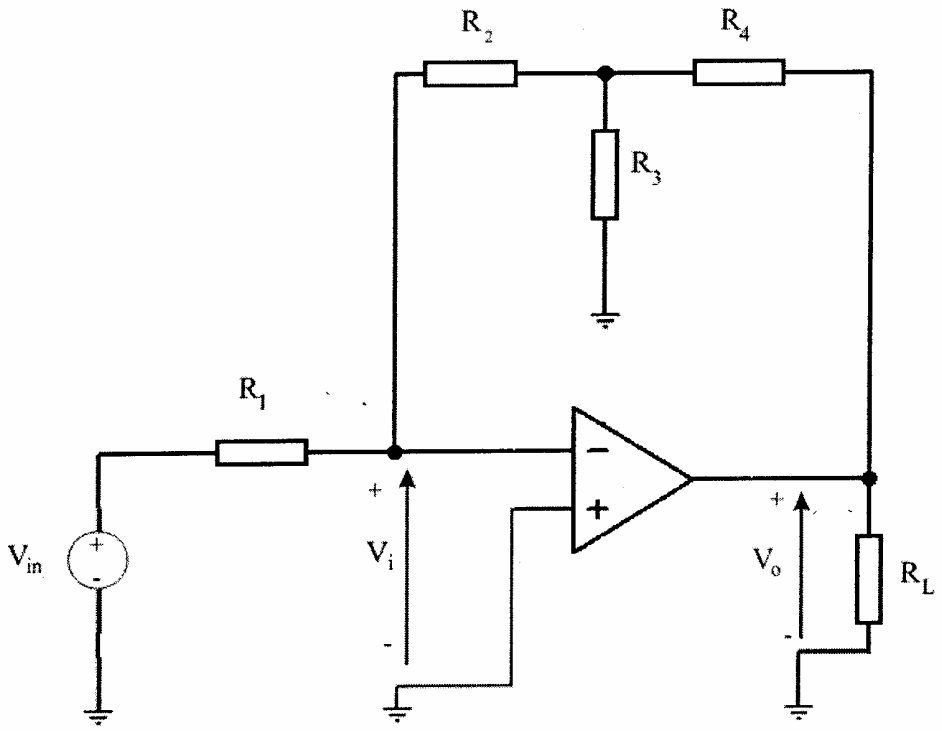

Figure Q.3 (b)

c) Calculate the overall voltage gain for the instrumentation amplifier in Figure Q.3 (c), where $v_1 = 10$ mV, $v_2 = 10$ mV, R =15kΩ, $R_1 = 150\Omega$, $R_2 = 33$kΩ. Also determine the current and voltage levels throughout the circuit when +1V common mode input (V_{CM}) is given along with the ±10 mV signals. Explain the voltage level at point A.

[8 marks]

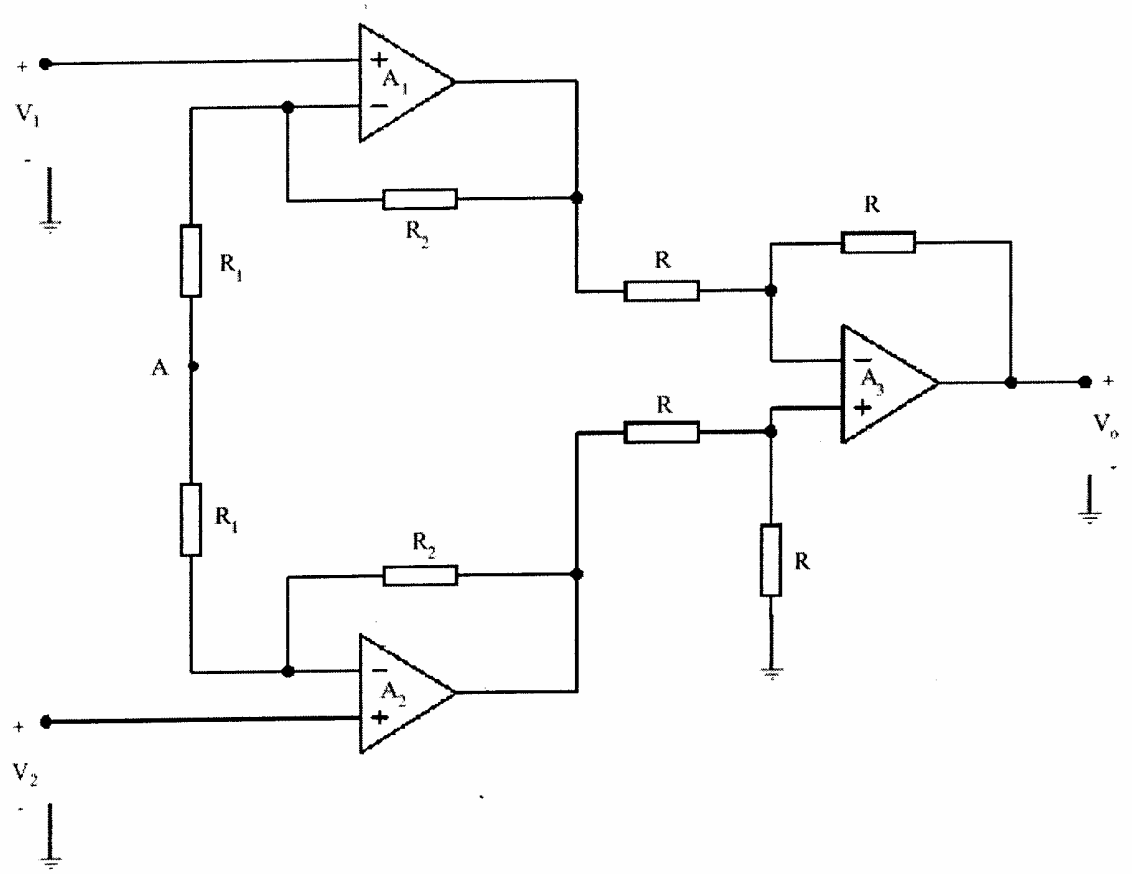

Figure Q.3 (c)

Question 04

a) Explain the selection of a Q-point on FET dc load line, and discuss the limitations on the output voltage swing.

[6 marks]

b) Draw the small-signal mid-band equivalent circuit to the given MOSFET amplifier circuit in Figure Q.4 (b). Assume that $r_d = \infty$ and derive expressions for the voltage gain, input resistance, output resistance and evaluate the expressions, where $R = 100k\Omega$, $R_f = 100k\Omega$, $R_D = 3k\Omega$, $R_L = 10k\Omega$, $V_{DD} = 20V$, $V_{to} = 5V$ and $K = 1mA/V^2$.

[8 marks]

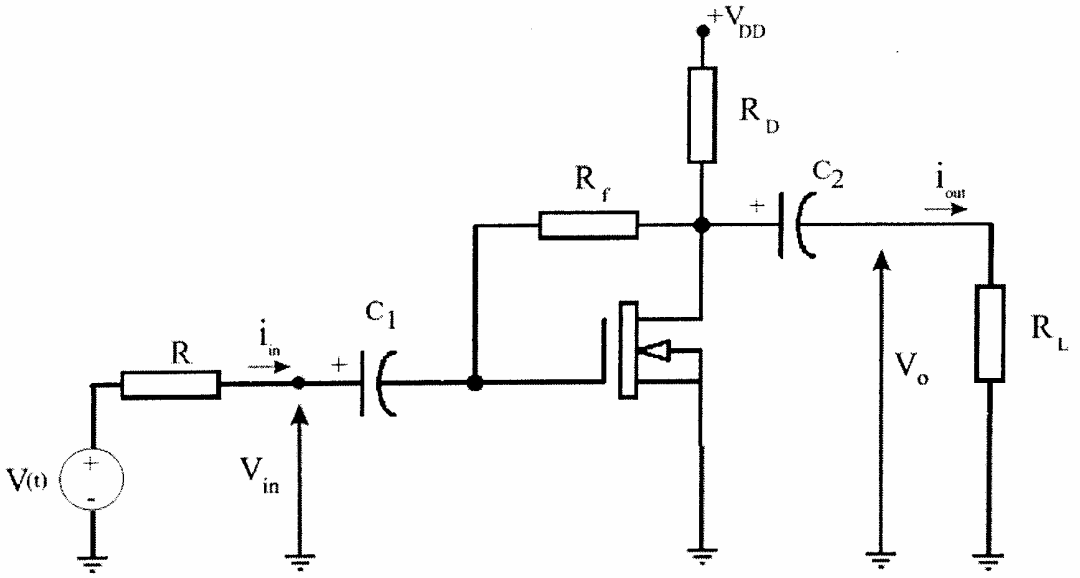

Figure Q.4 (b)

c) Find the values of g_m and r_d for the characteristics of Figure Q.4 (c) at a Q point of $V_{GSQ} = 2.5V$ and $V_{DSQ} = 6V$.

[6 marks]

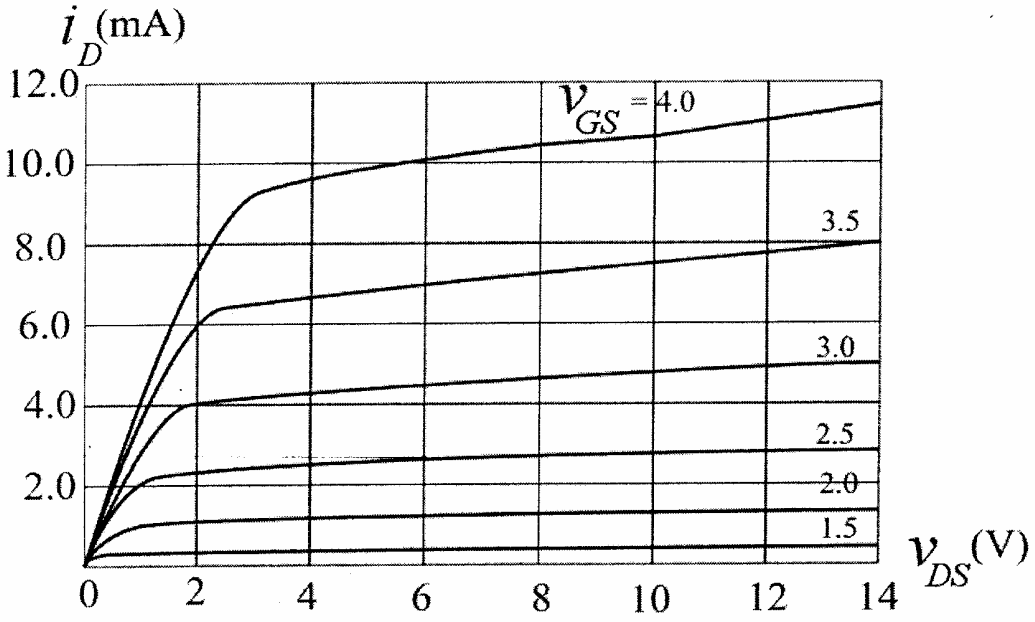

Figure Q.4 (c)

Question 05

a) Negative feedback is produced by feeding a portion of an amplifier output back to the input where it behaves as an additional signal. List at least two advantages of using negative feedback. Derive an equation for the overall voltage gain of the feedback amplifier shown in the Figure Q.5 (a), in which v_i is amplified to produce v_o. A_v and B represent open loop gain and feedback factor respectively.

[6 marks]

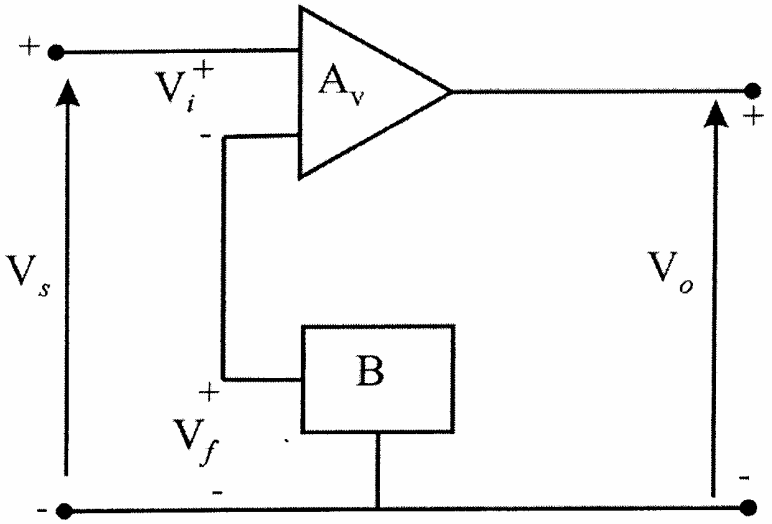

Figure Q.5 (a)

b) Calculate the closed-loop gain for the negative feedback amplifier shown in the Figure Q.5 (a). Also calculate the closed loop gain when the open-loop gain is changed by ±50%. Note that A_v = 100 000 and B = 1/100.

[6 marks]

c) The Wein bridge oscillator in Figure Q.5 (c) has the following components: $R_1 = R_2 = R_4 = 5.6k\Omega$, $R_3 = 12k\Omega$, $C_1 = C_2 = 2700pF$. Calculate the oscillating frequency.

[8 marks]

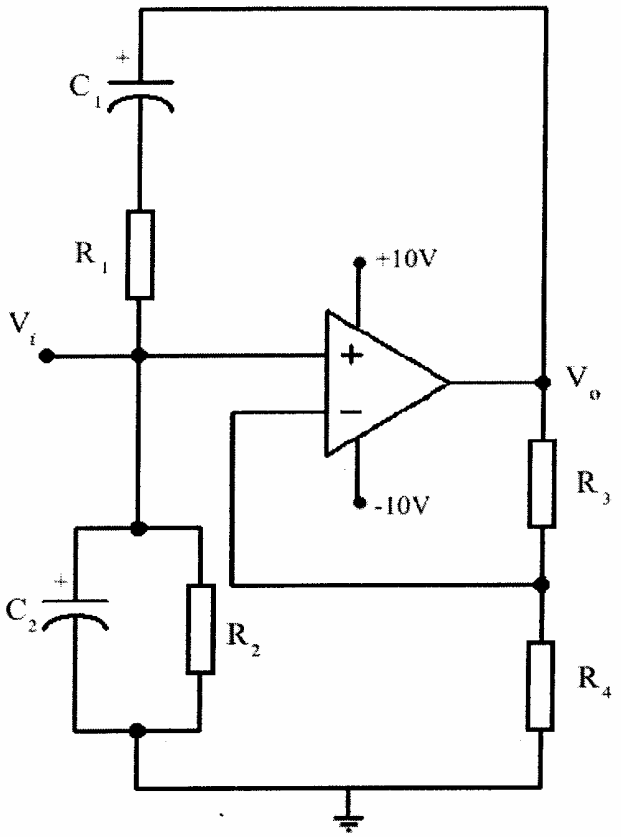

Figure Q.5 (c)

Question 06:

a) Describe programmable array logic (PAL) and Programmable logic array (PLA) devices.
[4 marks]

b) Using PAL, show how you can implement the minimized sum of product function for the following.

$$F(A,B,C,D) = \sum(0,1,2,3,7,8,9,11,12,15)$$

[8 marks]

c) Define Fan-out, Fan-in, and Propagation Delay. Given the network in below FigureQ.6(c), what is the worst case propagation delay?

$\Delta f_1 = 10ns$

$\Delta f_2 = 20ns$

$\Delta f_3 = 25ns$

$\Delta f_4 = 10ns$

[8 marks]

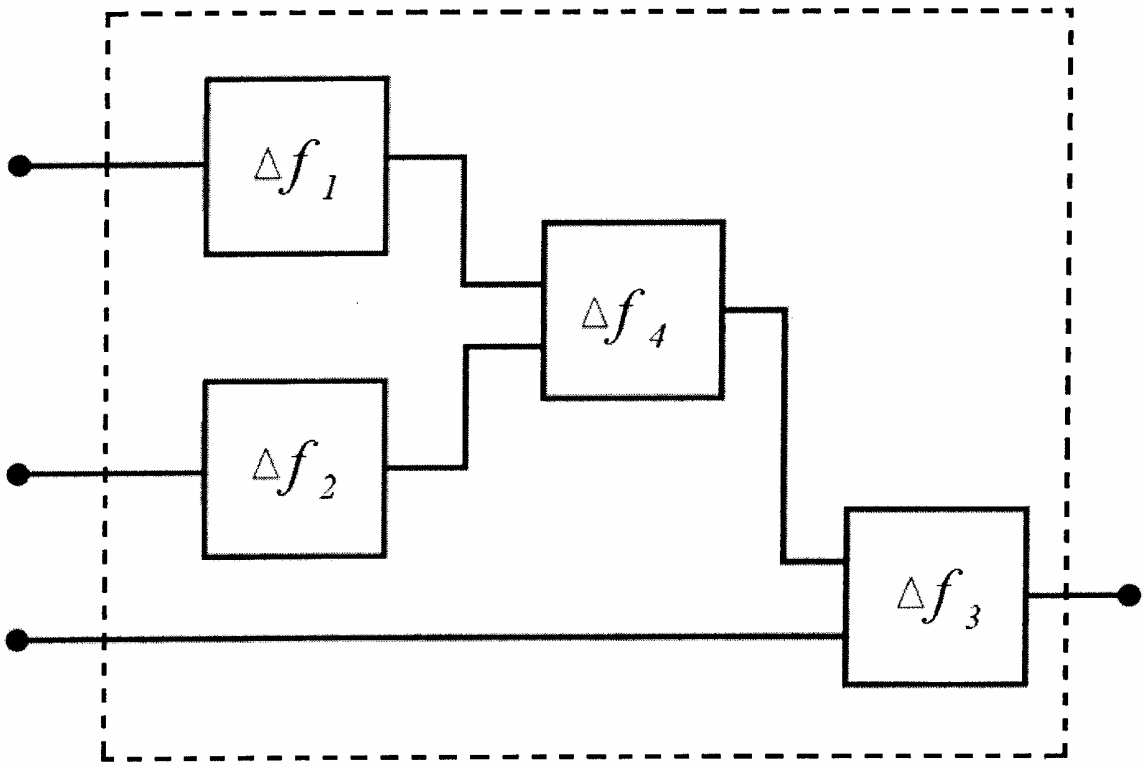

Figure Q.6 (c)

Question 07

a) Find the minimum sum of products (SOPs) and product of sums (POSs) form of the following functions using Karnaugh maps:

i. $F(A,B,C,D) = \sum(1,3,5,7,9,11)$

ii. $F(A,B,C,D) = \sum(5,7,9,10,11) + dc \cdot terms(2,13,15)$

(dc. terms = don't-care terms)

[6 marks]

b) Design a 2-bit full adder with minimum hardware using standard 2-input gates available in logic families. Clearly show the steps of your design.

[6 marks]

c) Implement the following logic function using a 4-input multiplexer with a minimum number of basic logic gates (AND, OR, NOT).

$F(A,B,C,D) = \sum(5,7,9,10,11) + dc \cdot terms(2,13,15)$

[8 marks]

Question 08

a) Carry out the following conversions.
   i. Convert a J-K Flip-Flop to a D Flip-Flop.
   ii. Convert a J-K Flip-Flop to a T Flip-Flop.

[4 marks]

b) A master-slave J-K flip-flop is shown in Figure Q.8 (b). Assuming that the initial condition of the flip-flop is J=K=$Q_m = Q_s = 0$, trace the logic levels through the diagram for the following changes (N.B. changes in J and K take place in the time intervals between clocks pulse).
   i. $J,0 \rightarrow 1; k,0 \rightarrow 0$ clock pulse 1 applied
   ii. $J,1 \rightarrow 0; k,0 \rightarrow 1$ clock pulse 2 applied
   iii. $J,0 \rightarrow 0; k,1 \rightarrow 0$ clock pulse 3 applied
   iv. $J,0 \rightarrow 1; k,0 \rightarrow 0$ clock pulse 4 applied

Draw a timing diagram displaying the J, K, Q_m, Q_s waveforms for the period of four clock pulses.

[8 marks]

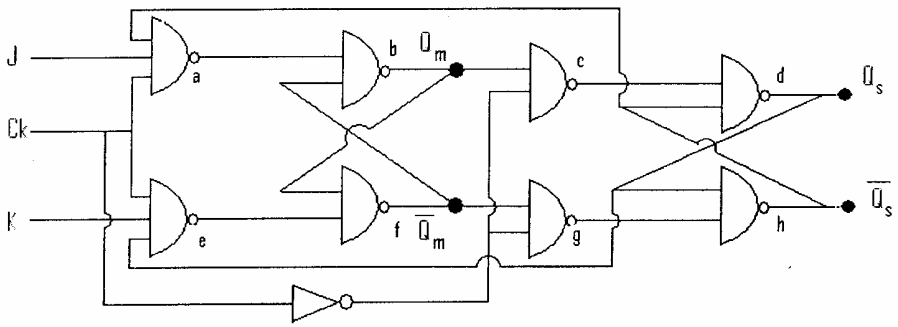

Figure Q.8 (b)

c) Design a decade counter using a four stage shift register having the following state sequence.
$0000 \rightarrow 0001 \rightarrow 0011 \rightarrow 0111 \rightarrow 1111 \rightarrow 1110 \rightarrow 1101 \rightarrow 1010 \rightarrow 0100 \rightarrow 1000$

[8 marks]